

SPECIFICATION

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INTEGRATED CIRCUIT PHASE PARTITIONED POWER DISTRIBUTION FOR STRESS POWER REDUCTION

Background of the Invention

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to the field of integrated circuits; more specifically, it relates to stressing of integrated circuits utilizing level sensitive scan design (LSSD.)

[0003] BACKGROUND OF THE INVENTION

[0004] Stress test modes are commonly used in modern synchronous integrated circuits to subject the integrated circuit to various types of tests that "stress" the circuit and are designed to cause reliability defects to fail during stress rather than later, in the field. One common stress type is called burn-in. During burn-in, the integrated circuit is subjected to high temperatures and higher than normal operational voltages in an effort to cause early drop out of the reliability defects.

[0005]

LSSD is a method of testing integrated circuits wherein scan latches are placed between logic circuits. The scan latches allow a test vector to be sequenced through the logic circuits so the output vector can be compared to an expected vector to determine if there has been a fail in any of the logic circuits. During stress testing, all the scan latches and logic circuits are powered. For very large and high-speed integrated circuit dies at the leading edge of device technology (i.e. advanced transistor design), sub threshold leakage currents have become significant. In many cases, the stress standby current for a test like burn-in can exceed the current

capability of the stress tester. Currents in excess of 75 amperes are routinely encountered. One alternative is to build higher current stress testers, but this is a very expensive solution, and earlier generations of stress testers would become obsolete. A more desirable solution would be to reduce the standby current draw of the integrated circuit during stress.

[0006] Thus, there is an unmet need in the art for a high speed, leading edge technology integrated circuit design that requires lower standby current during stress test.

Brief Description of the Several Views of the Drawings

[0007] BRIEF DESCRIPTION OF DRAWINGS

[0008] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

[0009] FIG. 1 is a schematic diagram of an integrated circuit die illustrating pad assignments according to the present invention;

[0010] FIG. 2 is a schematic diagram of an integrated circuit device according to a first embodiment of the present invention;

[0011] FIG. 3 is a schematic diagram of an alternative latching arrangement of the integrated circuit device of the first embodiment of the present invention;

[0012] FIG. 4 is a timing diagram for clock and power signals for the integrated circuit device of the first embodiment of the present invention;

[0013] FIG. 5 is a schematic diagram illustrating a stress tester and alternative methods of stressing an integrated circuit device according to the present invention;

[0014] FIG. 6 is a schematic diagram of an integrated circuit device according to a second embodiment of the present invention; and

[0015] FIG. 7 is a timing diagram for clock and power signals for the integrated circuit device of the second embodiment of the present invention.

Detailed Description of the Invention

[0016] DETAILED DESCRIPTION OF THE INVENTION

[0017] FIG. 1 is a schematic diagram of an integrated circuit die illustrating pad assignments according to the present invention. In FIG. 1, integrated circuit die 100, comprises a multiplicity of ground pads 105, VDD0 pads 110, VDD1 pads 115, VDD2 pads 120 and signal pads 125 disposed on a top surface of the integrated circuit die. About 50% of the pads are signal pads 125, about 25% are ground pads 105 and the rest are distributed among VDD0 pads 110, VDD1 pads 115 and VDD2 pads 120. The number of VDD1 pads 115 and VDD2 pads 120 are approximately equal. The number of VDD0 pads 110 is very much smaller than the number of VDD1 pads 115 and VDD2 pads 120. The exact distribution of pads is a function of circuit power and signal requirements in integrated circuit die 100. The number of total pads may exceed 4000.

[0018] VDD0 pads 110 are used to supply power to clocks on integrated circuit die 100. VDD1 pads 115 are used to supply power to approximately one half of the latches on integrated circuit die 100 and VDD2 pads 120 are used to supply power to the remaining latches the integrated circuit die. During normal operation VDD0 pads 110, VDD1 pads 115 and VDD2 pads 120 may be supplied from the same external power supply, however during stress, the VDD0, VDD1 and VDD2 pads are supplied from different power supplies that are controlled by the stress tool. The voltages applied to VDD1 pads 115 and VDD2 pads 120 during the stress are generally higher than applied during normal operation of integrated circuit die 100 but are generally equal to each other. However, there may be circumstances that applying different voltages to VDD1 pads 115 and VDD2 pads may be useful.

[0019] As illustrated, the VDD pads of integrated circuit die 100 are shown for a two-phase embodiment of the present invention, that is, a two-clock system. In a four-phase embodiment, a four-clock system, there would also be pads for supplying VDD3 and VDD4 voltages, the number of pads supplying VDD1, VDD2, VDD3 and VDD4 being approximately equal to one another. The first embodiment of the present invention is to a two-clock system. The second embodiment of the present invention is to a four-clock system.

[0020] FIG. 2 is a schematic diagram of an integrated circuit device according to a first embodiment of the present invention. In FIG. 2, an integrated circuit device 140 comprises a series of alternating L1 latches 145 and L2 latches 150 interspersed with logic circuits 155A and 155B. Logic circuits 155A and 155B may comprise one or more logic gates arranged sequentially. Logic circuits 155A are coupled between the output of L1 latches 145 and the input of L2 latches 150. Logic circuits 155B are coupled between the output of L2 latches 150 and the input of L1 latches 145. Each L1 latch 145 is powered from a VDD1 power rail, as is each logic circuit 155A. Each L2 latch 150 is powered from a VDD2 power rail, as is each logic circuit 155B. Each of logic circuits 155A is not intended to be identical; (though they may be identical) they are merely powered from the same VDD1 power rail. Each of logic circuits 155B is not intended to be identical; (though they may be identical) they are merely powered from the same VDD2 power rail. Each L1 latch 145 is clocked by a C1 clock 160. Each L2 latch 150 is clocked by a C2 clock 165. Both C1 clock 160 and C2 clock 165 are powered from a VDD0 power rail.

[0021] During stress, when C1 clock 160 is high, C2 clock 165 is low, VDD1 is high, VDD2 is low, all L1 latches 145 are powered and all L2 latches 150 are de-powered. Data in logic circuits 155B is latched by L1 latches 145. Data in logic circuits 155A cannot be latched by L2 latches 150 since all the L2 latches are de-powered. Only L1 latches 145 and logic circuits 155A are drawing current when C1 clock 160 is high.

[0022] When C1 clock 160 is low, C2 clock 165 is high, VDD1 is low, VDD2 is high, all L1 latches 145 are de-powered and all L2 latches 150 are powered. Data in logic circuits 155A is latched by L2 latches 150. Data in logic circuits 155B cannot be latched by L1 latches 145 since all the L1 latches are de-powered. Only L2 latches 150 and logic circuits 155B are drawing current when C2 clock 165 is high. Therefore, half the current normally required for stressing a conventional logic circuit is required when integrated circuit device 140 is stressed.

[0023] There is a requirement of some overlap in VDD1 and VDD2 in order to gate data from and to L1 latches 145 and from and to L2 latches 150. This is illustrated in FIG. 4 and described below.

[0024] FIG. 3 is a schematic diagram of an alternative latching arrangement of the

integrated circuit device of the first embodiment of the present invention. In FIG. 3, an integrated circuit device 170 comprises a first set of logic circuits 175 and a second set of logic circuits 180. First set of logic circuits 175 comprises a series of L1/L2 latches 185 alternating with logic circuits 155B. Each L1/L2 latch 185 comprises one L1 latch 145 directly feeding one L2 latch 150. For L1/L2 latches 185, L1 latch 145 is a master latch and L2 latch 150 is a slave latch. Logic circuits 155B are coupled between the output of each L2 150 latch and the input of each L1 latch 145. Second set of logic circuits 180 comprises a series of L2/L1 latches 190 alternating with logic circuits 155A. Each L2/L1 latch 190 comprises one L2 latch 150 directly feeding one L1 latch 145. For L2/L1 latches 190, L2 latch 150 is a master latch and L1 latch 145 is a slave latch. Logic circuits 155A are coupled between the output of each L1 latch 145 and the input of each L2 latch 150. Each L1 latch 145 is powered from a VDD1 power rail, as is each logic circuit 155A. Each L2 latch 150 is powered from a VDD2 power rail. Each L1 latch 145 is clocked by C1 clock 160. Each L2 latch 150 is clocked by C2 clock 165. Both C1 clock 160 and C2 clock 165 are powered from a VDD0 power rail.

[0025] During stress, when C1 clock 160 is high, C2 clock 165 is low, VDD1 is high, VDD2 is low, all L1 latches 145 are powered and all L2 latches 150 are de-powered. In first set of logic circuits 175, data in logic circuits 155B is latched by L1 latches 145. Data in L1 latches 145 cannot be latched by L2 latches 150 since all the L2 latches are de-powered. Only L1 latches 145 are drawing power. In second set of logic circuits 180, data in logic latches 150 is latched by L1 latches 145. Data in logic circuits 155A cannot be latched by L2 latches 150 since all the L2 latches are de-powered. Only L1 latches 145 and logic circuits 155A are drawing current.

[0026] When C1 clock 160 is low, C2 clock 165 is high, VDD1 is low, VDD2 is high, all L1 latches 145 are de-powered and all L2 latches 150 are powered. In first set of logic circuits 175, data in L1 latches 145 is latched by L2 latches 150. Data in logic circuits 155B cannot be latched by L1 latches 145 since all the L1 latches are de-powered. Only L2 latches 145 and logic circuits 155B are drawing power when C1 clock 160 is high. In second set of logic circuits 180, data in logic latches logic circuits 155A is latched by L2 latches 150. Data in logic L2 latches 150 cannot be latched by L1 latches 145 since all the L1 latches are de-powered. Only L2 latches 150 and logic circuits 155A are drawing current when C2 clock 165 is high. Therefore, half the

current normally required for stressing a conventional logic circuit is required when integrated circuit device 170 is stressed.

[0027] Again, there is a requirement of some overlap in VDD1 and VDD2 in order to gate data from and to L1 latches 145 and from and to L2 latches 150. This is illustrated in FIG. 4 and described below.

[0028] FIG. 4 is a timing diagram for clock and power signals for the integrated circuit device of the first embodiment of the present invention. In FIG. 4, the relationship between the phases of the C1 and C2 clocks, VDD0 and the rise and fall of VDD1 and VDD2 is illustrated. C1 is high only during periods "P1." C2 is high only during periods "P2." C1 and C2 are never high in the same period and do not overlap. The duration of periods "P1" may equal "P2." In one example, the C1 and C2 clock frequencies are about five MHz. VDD0 is always high as it is the clock power supply. VDD1 rises \hat{t}_1 before C1 goes high and falls \hat{t}_2 after C1 goes low. VDD2 rises \hat{t}_3 before C2 goes high and falls \hat{t}_4 after C2 goes low. \hat{t}_1 , \hat{t}_2 , \hat{t}_3 and \hat{t}_4 may be equal.

[0029] FIG. 5 is a schematic diagram illustrating a stress tester and alternative methods of stressing an integrated circuit device according to the present invention. In FIG. 5, stress tester 195 comprises a stress control unit 200 and a stress chamber 205. Stress control unit 200 is linked by a signal/power cable 210A to whole wafer stress fixture 215 or by a signal/power cable 210B to one or more die stress fixtures 220 or by a signal/power cable 210C to a module stress fixture 225.

[0030] Whole wafer stress fixture 215 comprises a wafer chuck 230 for holding an undiced integrated circuit wafer 235 and a test head 240 having a multiplicity of probes 245 for contacting pads on wafer 235.

[0031] Die stress fixtures 220 comprise a die holder 250 for holding an integrated circuit die 255, a test head 260 having a multiplicity of probes 265 for contacting pads on integrated circuit die 255 and locking mechanisms 270 for holding test head 260 in place.

[0032] Module stress fixture 225 comprises a stress board 275 having a multiplicity of sockets 280. Sockets 280 are adapted to receive pins 285 of modules 290. Each

module 290 contains one or more integrated circuit dies 295.

[0033] C1, C2, VDD0, VDD1, VDD2 (also C3, C4, VDD3 and VDD4 of the second embodiment illustrated in FIGs. 6 and 7 and described below) as well as any data signals are controlled by stress control unit 200. Stress chamber 205 is capable of temperature and humidity control. In one example, VDD1, VDD2, VDD3 and VDD4 are 1.5 times the normal operational voltage of the integrated circuit wafer, die or module being stressed and the temperature is controlled to either 140oC or 180oC.

[0034] FIG. 6 is a schematic diagram of an integrated circuit device according to a second embodiment of the present invention. In FIG. 6, an integrated circuit device 300 comprises a series of alternating L1 latches 305, L2 latches 310, L3 latches 315 and L4 latches 320 interspersed with logic circuits 325A, 325B, 325C and 325D. Logic circuits 325A are coupled between the output of each L1 latch 305 and the input of each L2 latch 310. Logic circuits 325B are coupled between the output of each L2 latch 310 and the input of each L3 latch 315. Logic circuits 325C are coupled between the output of each L3 latch 315 and the input of each L4 latch 320. Logic circuits 325D are coupled between the output of each L4 latch 320 and the input of each L1 latch 305. Each L1 latch 305 is powered from a VDD1 power rail, as is each logic circuit 325A. Each L2 latch 310 is powered from a VDD2 power rail, as is each logic circuit 325B. Each L3 latch 315 is powered from a VDD3 power rail, as is each logic circuit 325C. Each L4 latch 320 is powered from a VDD4 power rail, as is each logic circuit 325D. Each of logic circuits 325A is not intended to be identical; (though they may be identical) they are merely powered from the same VDD1 power rail. Each of logic circuits 325B is not intended to be identical; (though they may be identical) they are merely powered from the same VDD1 power rail. Each of logic circuits 325C is not intended to be identical (though they may be identical); they are merely powered from the same VDD3 power rail. Each of logic circuits 325D is not intended to be identical; (though they may be identical) they are merely powered from the same VDD4 power rail. Each L1 latch 305 is clocked by a C1 clock 330. Each L2 latch 310 is clocked by a C2 clock 335. Each L3 latch 315 is clocked by a C3 clock 340. Each L4 latch 320 is clocked by a C4 clock 340. C1 clock 330, C2 clock 335, C3 clock 340 and C4 clock 345 are powered from a VDD0 power rail.

- [0035] During stress, when C1 clock 330 is high, C2 clock 335, C3 clock 340 and C4 clock 345 are low, VDD1 is high, VDD2, VDD3 and VDD4 are off, all L1 latches 305 are powered and all L2 latches 310, L3 latches 315 and L4 latches 320 are de-powered. Data in logic circuits 325D is latched by L1 latches 305. Data in logic circuits 325A, logic circuits 325B and logic circuits 325C cannot be latched by L2 latches 310, L3 latches 315 and L4 latches 320 respectively, since only the L1 latches are powered. Only L1 latches 305 and logic circuits 325A are drawing current when C1 clock 330 is high.
- [0036] When C2 clock 335 is high, C1 clock 330, C3 clock 340 and C4 clock 345 are off, VDD2 is high, VDD1, VDD3 and VDD4 are off, all L2 latches 310 are powered and all L1 latches 305, L3 latches 315 and L4 latches 320 are de-powered. Data in logic circuits 325A is latched by L2 latches 310. Data in logic circuits 325B, logic circuits 325C and logic circuits 325D cannot be latched by L3 latches 315, L4 latches 320 and L1 latches 305 respectively, since only the L2 latches are powered. Only L2 latches 310 and logic circuits 325B are drawing current when C2 clock 335 is high.
- [0037] When C3 clock 340 is high, C1 clock 330, C2 clock 335 and C4 clock 345 are off, VDD3 is high, VDD1, VDD2 and VDD4 are off, all L3 latches 315 are powered and all L1 latches 305, L2 latches 310 and L4 latches 320 are de-powered. Data in logic circuits 325B is latched by L3 latches 315. Data in logic circuits 325D, logic circuits 325A and logic circuits 325C cannot be latched by L1 latches 305, L2 latches 310 and L4 latches 320 respectively, since only the L3 latches are powered. Only L3 latches 315 and logic circuits 325C are drawing current when C3 clock 340 is high.
- [0038] When C4 clock 345 is high, C1 clock 330, C2 clock 335 and C3 clock 340 are off, VDD4 is high, VDD1, VDD2 and VDD3 are off, all L4 latches 320 are powered and all L1 latches 305, L2 latches 310 and L3 latches 315 are de-powered. Data in logic circuits 325C is latched by L4 latches 320. Data in logic circuits 325D, logic circuits 325A and logic circuits 325B cannot be latched by L1 latches 305, L2 latches 310 and L3 latches 315 respectively, since only the L4 latches are powered. Only L4 latches 320 and logic circuits 325D are drawing current when C4 clock 345 is high. Therefore, a quarter of the current normally required for stressing a conventional logic circuit is required when integrated circuit device 300 is stressed.

[0039] There is a requirement of some overlap of VDD1 and VDD2 and of VDD3 and VDD4 in order to gate data from and to L1 latches 305 and L2 latches 310 and from and to L3 latches 315 and L4 latches 320 respectively. This is illustrated in FIG. 7 and described below.

[0040] FIG. 7 is a timing diagram for clock and power signals for the integrated circuit device of the second embodiment of the present invention. FIG. 7 shows the relationship between the phases of the C1, C2, C3 and C4 clocks, VDD0 and the rise and fall of VDD1, VDD2, VDD3 and VDD4. C1 is high only during periods "P1." C2 is high only during periods "P2." C3 is high only during periods "P3." C4 is high only during periods "P4." C1, C2, C3 and C4 are never high in the same period and do not overlap. The duration of time periods "P1", "P2", "P4" and "P2" may be equal to each other. In one example, the C1, C2, C3 and C2 clock frequencies are about five MHz. VDD0 is always high as it is the clock power supply. VDD1 rises \hat{t}_1 before C1 goes high and falls \hat{t}_2 after C1 goes low. VDD2 rises \hat{t}_3 before C2 goes high and falls \hat{t}_4 after C2 goes low. VDD3 rises \hat{t}_5 before C3 goes high and falls \hat{t}_6 after C3 goes low. VDD4 rises \hat{t}_7 before C4 goes high and falls \hat{t}_8 after C4 goes low. \hat{t}_1 , \hat{t}_2 , \hat{t}_3 , \hat{t}_4 , \hat{t}_5 , \hat{t}_6 , \hat{t}_7 and \hat{t}_8 may be equal.

[0041] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.